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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,018	03/11/2004	Junichi Hikita	AI 257 D1	3920

7590 07/12/2005

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,018	HIKITA ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5,6 and 2122* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/499,384.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Invention of Figures 5-9, Claims 5, 6, 21 and 22, in the reply filed on 05/17/05 is acknowledged.

Claim Objections

2. Claims 6 and 22 are objected to because of the following informalities: In claims 6 and 22, line 1, "A" should be changed to "The" for clarity. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 5, 6, 21 and 22 rejected under 35 U.S.C. 102(b) as being anticipated by Takao (JP 58-091646, of record).

Takao discloses, as shown in Figures 1, 2, 6 and 7, a semiconductor chip, comprising

a semiconductor substrate (1) having a low impedance portion (2);

a functional bump (3a) provided on a surface of the semiconductor substrate for electrical connection between an internal circuit provided on the semiconductor substrate and a solid device (3);

a dummy bump (5") provided on the surface of the semiconductor substrate and not serving for electrical connection between the internal circuit and the solid device yet electrically connected to the low impedance portion of the semiconductor substrate,

wherein the functional bump is provided on a peripheral portion of a mating surface of the semiconductor chip opposed to the solid device,

wherein the dummy bump is provided on a central portion of the mating surface.

Regarding claims 6 and 22, Takao discloses the dummy bumps has a greater connect area in contact with the solid device than the functional bump.

Regarding claim 6, Takao discloses, , as shown in Figures 1, 2, 6 and 7, a semiconductor, comprising:

a solid device (1);

a semiconductor chip (3) mounted and bonded onto a surface of the solid device;

a functional bump (3a) for electrical connection between an internal circuit of the semiconductor chip and the solid device;

a dummy bump (5") not serving for electrical connection between the internal circuit and the solid device wherein at least one of the solid device and the semiconductor chip includes a low impedance portion and the dummy bump is electrically connected to the low impedance portion,

wherein the functional bump is disposed in association with a peripheral portion of a mating surface of the semiconductor chip opposed to the solid device, and

wherein the dummy bump is disposed in association.

4. Claims 5 and 21 rejected under 35 U.S.C. 102(a) as being anticipated by Yano et al. (PN 5,909,058).

Yano et al. discloses, as shown in Figures 1-6, a semiconductor chip, comprising

a semiconductor substrate (20) having a low impedance portion (not shown);

a functional bump (13a) provided on a surface of the semiconductor substrate for electrical connection between an internal circuit provided on the semiconductor substrate and a solid device (3);

a dummy bump (13b) provided on the surface of the semiconductor substrate and not serving for electrical connection between the internal circuit and the solid device yet electrically connected to the low impedance portion of the semiconductor substrate,

wherein the functional bump is provided on a peripheral portion of a mating surface of the semiconductor chip opposed to the solid device,

wherein the dummy bump is provided on a central portion of the mating surface.

Regarding claim 21, Yano et al. discloses, as shown in Figures 1-6, a semiconductor, comprising:

a solid device (20);

a semiconductor chip (14) mounted and bonded onto a surface of the solid device;

a functional bump (3a) for electrical connection between an internal circuit of the semiconductor chip and the solid device;

a dummy bump (13b) not serving for electrical connection between the internal circuit and the solid device wherein at least one of the solid device and the semiconductor chip includes a low impedance portion and the dummy bump is electrically connected to the low impedance portion,

wherein the functional bump is disposed in association with a peripheral portion of a mating surface of the semiconductor chip opposed to the solid device, and

wherein the dummy bump is disposed in association.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

June 24, 2005

Hung Vu

Primary Examiner